L Number	Hits	Search Text	DB	Time stamp
-	1	("6549963").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 11:08
-	24	riffault-$.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 12:50
-	1	6275240.URPN.	USPAT	2003/07/01 12:38
-	9	(capacit$5 or loading) same (strobe adj3 signal$1)same compliment$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 13:25
-	42	(capacitive or capacitance or capacitor) near5 loading near5 balanc$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 13:45
-	2	((capacitive or capacitance or capacitor) near5 loading near5 balanc$3) same (bus or busses or buses)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 13:50
-	324	(bus near3 signal$1) same balanc$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/01 13:59
-	39	(bus near3 signal$1) same load$3 same balanc$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 10:12
-	6	("3622708" | "3991279" | "3991280" | "4090043" | "4146753" | "4301336").PN.	USPAT	2003/07/02 10:11
-	2	5054062.URPN.	USPAT	2003/07/02 10:12
-	2	("6029216").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 10:13
-	1152	326/30.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 10:13
-	66	agp same terminat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:47
-	4	("4749877" | "5490117" | "5613130" | "5973416").PN.	USPAT	2003/07/02 10:58
-	5502	bus near5 terminat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:48

-	41353	upgrad$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:48
-	11	(bus near5 terminat$4) same upgrad$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:48
-	5	("5799204" | "5884053" | "5892964" | "6141021" | "6170029").PN.	USPAT	2003/07/02 14:09
-	3	terminat$4 near10 (compliment$3 near5 signal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/09 17:19
-	85	buffer$4 near10 (compliment$3 near5 signal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/09 17:19
-	5	(buffer$4 near10 (compliment$3 near5 signal$1)) same (bus or busses or buses)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/09 17:20

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1 VIZARD—visualization accelerator for realtime display

Günter Knittel, Wolfgang Straßer

August 1997 **Proceedings of the 1997 SIGGRAPH/Eurographics workshop on Graphics hardware**

Full text available: pdf(931.67 KB) Additional Information: full citation, references, citings, index terms

Keywords: PCI-coprocessor, volume rendering accelerator

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Relevance scale

1 Evaluation of high performance multicache parallel texture mapping
Alexis Vartanian, Jean-Luc Béchennec, Nathalie Drach-Temam
July 1998 **Proceedings of the 12th international conference on Supercomputing**
Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

2 Rendering systems on clusters: Design and implementation of a large-scale hybrid distributed graphics system
Jian Yang, Jiaoying Shi, Zhefan Jin, Hui Zhang
September 2002 **Proceedings of the Fourth Eurographics Workshop on Parallel Graphics and Visualization**
Full text available: pdf(237.87 KB) Additional Information: full citation, abstract, references, index terms

Although modern graphics hardware has strong capability to render millions of triangles within a second, huge scenes are still unable to be rendered in real-time. Lots of parallel and distributed graphics systems are explored to solve this problem. However none of them is built for large-scale graphics applications.We designed AnyGL, a large-scale hybrid distributed graphics system, which consists of four types of logical nodes, Geometry Distributing Node, Geometry Rendering Node, Image Composit ...

Keywords: geometry compression, global share, image composition, image compression, large-scale cluster rendering, logical timestamp, memory explosion, parallel rendering, remote graphics, tiled displays, virtual graphics

3 Pomegranate: a fully scalable graphics architecture
Matthew Eldridge, Homan Igehy, Pat Hanrahan
July 2000 **Proceedings of the 27th annual conference on Computer graphics and interactive techniques**
Full text available: pdf(508.39 KB) Additional Information: full citation, abstract, references, citings, index terms

Pomegranate is a parallel hardware architecture for polygon rendering that provides scalable input bandwidth, triangle rate, pixel rate, texture memory and display bandwidth while maintaining an immediate-mode interface. The basic unit of scalability is a single graphics pipeline, and up to 64 such units may be combined. Pomegranate's scalability is achieved with a novel "sort-everywhere" architecture that distributes work in a balanced fashion at every stage of the pipeline, ke ...

Keywords: graphics hardware, parallel computing

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4 Hybrid sort-first and sort-last parallel rendering with a cluster of PCs

Rudrajit Samanta, Thomas Funkhouser, Kai Li, Jaswinder Pal Singh

August 2000 **Proceedings 2000 SIGGRAPH/EUROGRAPHICS workshop on on Graphics hardware**

Full text available: pdf(613.08 KB) Additional Information: full citation, abstract, references, citings, index terms

We investigate a new hybrid of sort-first and sort-last approach for parallel polygon rendering, using as a target platform a cluster of PCs. Unlike previous methods that statically partition the 3D model and/or the 2D image, our approach performs dynamic, view-dependent and coordinated partitioning of both the 3D model and the 2D image. Using a specific algorithm that follows this approach, we show that it performs better than previous approaches and scales better with both processor count ...

Keywords: cluster computing, parallel rendering

5 Sort-last parallel rendering: Sort-last parallel rendering for viewing extremely large data sets on tile displays

Kenneth Moreland, Brian Wylie, Constantine Pavlakos

October 2001 **Proceedings of the IEEE 2001 symposium on parallel and large-data visualization and graphics**

Full text available: pdf(2.14 MB) Additional Information: full citation, abstract, references, citings, index terms

Due to the impressive price-performance of today's PC-based graphics accelerator cards, Sandia National Laboratories is attempting to use PC clusters to render extremely large data sets in interactive applications. This paper describes a sort-last parallel rendering system running on a PC cluster that is capable of rendering enormous amounts of geometry onto high-resolution tile displays by taking advantage of the spatial coherency that is inherent in our data. Furthermore, it is capable of scal ...

Keywords: Compositing, PC-Cluster, Parallel Rendering, Sort-Last, Tile Display

6 GI-cube: an architecture for volumetric global illumination and rendering

Frank Dachille, Arie Kaufman

August 2000 **Proceedings 2000 SIGGRAPH/EUROGRAPHICS workshop on on Graphics hardware**

Full text available: pdf(650.91 KB) Additional Information: full citation, abstract, references, citings, index terms

The power and utility of volume rendering is increased by global illumination. We present a hardware architecture, GI-Cube, designed to accelerate volume rendering, empower volumetric global illumination, and enable a host of ray-based volumetric processing. The algorithm reorders ray processing based on a partitioning of the volume. A cache enables efficient processing of coherent rays within a hardware pipeline. We study the flexibility and performance of this new architecture using both ...

Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing

7 The WarpEngine: an architecture for the post-polygonal age

Voicu Popescu, John Eyles, Anselmo Lastra, Joshua Steinhurst, Nick England, Lars Nyland

July 2000 **Proceedings of the 27th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(298.54 KB) Additional Information: full citation, abstract, references, citings, index terms

We present the WarpEngine, an architecture designed for real-time imaged-based rendering of natural scenes from arbitrary viewpoints. The modeling primitives are real-world images with per-pixel depth. Currently they are acquired and stored off-line; in the near future real-time depth-image acquisition will be possible, the WarpEngine is designed to render in immediate mode from such data sources. The depth-image resolution is locally adapted by interpolation to match the resolut ...

Keywords: graphics hardware, image-based rendering

8 Ray tracing vs. scan conversion: The ray engine

Nathan A. Carr, Jesse D. Hall, John C. Hart

September 2002 **Proceedings of the conference on Graphics hardware 2002**

Full text available: pdf(1.88 MB) Additional Information: full citation, abstract, references, citings, index terms

Assisted by recent advances in programmable graphics hardware, fast rasterization-based techniques have made significant progress in photorealistic rendering, but still only render a subset of the effects possible with ray tracing. We are closing this gap with the implementation of ray-triangle intersection as a pixel shader on existing hardware. This GPU ray-intersection implementation reconfigures the geometry engine into a ray engine that efficiently intersects caches of rays for a wide varie ...

Keywords: hardware acceleration, pixel shaders, ray caching, ray classification, ray coherence, ray tracing

9 Neon: a single-chip 3D workstation graphics accelerator

Joel McCormack, Robert McNamara, Christopher Gianos, Larry Seiler, Norman P. Jouppi, Ken Correll

August 1998 **Proceedings of the 1998 EUROGRAPHICS/SIGGRAPH workshop on Graphics hardware**

Full text available: pdf(1.58 MB) Additional Information: full citation, references, citings, index terms

Keywords: chunk rendering, direct rendering, graphics pipeline, level of detail, rasterization, texture cache, tile rendering

10 Hardware accelerated rendering of antialiasing using a modified a-buffer algorithm

Stephanie Winner, Mike Kelley, Brent Pease, Bill Rivard, Alex Yen

August 1997 **Proceedings of the 24th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(113.06 KB) Additional Information: full citation, references, citings, index terms

Keywords: antialiasing, image partitioning, plane equation evaluation, scanline, texture mapping, transparency

11 Ray tracing vs. scan conversion: SaarCOR: a hardware architecture for ray tracing

Jörg Schmittler, Ingo Wald, Philipp Slusallek

September 2002 **Proceedings of the conference on Graphics hardware 2002**

Full text available: pdf(5.23 MB) Additional Information: full citation, abstract, references, citings, index terms

The ray tracing algorithmis well-known for its ability to generate high-quality images and its flexibility to support advanced rendering and lighting effects. Interactive ray tracing has been shown to work well on clusters of PCs and supercomputers but direct hardware support

for ray tracing has been difficult to implement.In this paper, we present a new, scalable, modular, and highly efficient hardware architecture for real-time ray tracing. It achieves high performance with extremely low memor ...

12 Intel MMX for multimedia PCs
Alex Peleg, Sam Wilkie, Uri Weiser
January 1997 **Communications of the ACM**, Volume 40 Issue 1
Full text available: pdf(3.15 MB) Additional Information: full citation, references, citings, index terms, review

13 Unstructured grids: Tetrahedral projection using vertex shaders
Brian Wylie, Kenneth Moreland, Lee Ann Fisk, Patricia Crossno
October 2002 **Proceedings of the 2002 IEEE symposium on Volume visualization and graphics**
Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, index terms

Projective methods for volume rendering currently represent the best approach for interactive visualization of unstructured data sets. We present a technique for tetrahedral projection using the programmable *vertex shaders* on current generation commodity graphics cards. The technique is based on Shirley and Tuchman's Projected Tetrahedra (PT) algorithm and allows tetrahedral elements to be volume scan converted within the graphics processing unit. Our technique requires no pre-processing ...

Keywords: PC graphics hardware, direct volume rendering, projection volume rendering, volume scan conversion

14 Optimizing the data cache performance of a software MPEG-2 video decoder
Peter Soderquist, Miriam Leeser
November 1997 **Proceedings of the fifth ACM international conference on Multimedia**
Full text available: pdf(1.76 MB) Additional Information: full citation, references, citings, index terms

15 Design of a high performance volume visualization system
Barthold Lichtenbelt
August 1997 **Proceedings of the 1997 SIGGRAPH/Eurographics workshop on Graphics hardware**
Full text available: pdf(1.11 MB) Additional Information: full citation, references, citings, index terms

Keywords: OpenGL, system design, visualization, volume accelerator, volume rendering

16 Design space exploration and architectural design of HW/SW systems: Metrics for design space exploration of heterogeneous multiprocessor embedded systems
Donatella Sciuto, Fabio Salice, Luigi Pomante, William Fornaciari
May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**
Full text available: pdf(633.95 KB) Additional Information: full citation, abstract, references

This paper considers the problem of designing heterogeneous multiprocessor embedded systems. The focus is on a step of the design flow: the definition of innovative metrics for the analysis of the system specification to statically identify the most suitable processing elements class for each system functionality. Experimental results are also included, to show the applicability and effectiveness of the proposed methodology.

Keywords: heterogeneous multiprocessor Embedded Systems, metrics for Hw/Sw

partitioning, system-level design

17 Specialized architectures for structured volume rendering: Parallel volume rendering on a single-chip SIMD architecture

M. Meißner, S. Grimm, W. Straßer, J. Packer, D. Latimer

October 2001 **Proceedings of the IEEE 2001 symposium on parallel and large-data visualization and graphics**

Full text available: pdf(438.37 KB) Additional Information: full citation, abstract, references, index terms

Volume rendering has great potential for parallelization due to the tremendous number of computations necessary. Besides the enormous computational power needed, the memory interface is usually of crucial importance and frequently the bottleneck.This paper presents an implementation of a parallel ray casting algorithm for orthogonal projections on a new single-chip SIMD architecture. Concurrent processing of rays is scheduled such that redundant memory accesses of the individual processing eleme ...

Keywords: Parallel Processing, Ray Casting, Volume Rendering

18 Rendering and simulation: Physically-based visual simulation on graphics hardware

Mark J. Harris, Greg Coombe, Thorsten Scheuermann, Anselmo Lastra

September 2002 **Proceedings of the conference on Graphics hardware 2002**

Full text available: pdf(2.65 MB) Additional Information: full citation, abstract, references

In this paper, we present a method for real-time visual simulation of diverse dynamic phenomena using programmable graphics hardware. The simulations we implement use an extension of cellular automata known as the coupled map lattice (CML). CML represents the state of a dynamic system as continuous values on a discrete lattice. In our implementation we store the lattice values in a texture, and use pixel-level programming to implement simple next-state computations on lattice nodes and their nei ...

Keywords: CML, coupled map lattice, graphics hardware, multipass rendering, reaction-diffusion, visual simulation

19 Shader-driven compilation of rendering assets

Paul Lalonde, Eric Schenk

July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 3

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, index terms

Rendering performance of consumer graphics hardware benefits from pre-processing geometric data into a form targeted to the underlying API and hardware. The various elements of geometric data are then coupled with a shading program at runtime to draw the asset.In this paper we describe a system in which pre-processing is done in a compilation process in which the geometric data are processed with knowledge of their shading programs. The data are converted into structures targeted directly to the ...

Keywords: computer games, graphics systems, rendering, rendering systems

20 Watertight tessellation using forward differencing

Henry Moreton

August 2001 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on on Graphics hardware**

Full text available: pdf(28.78 MB) Additional Information: full citation, abstract, references, index terms

In this paper we describe an algorithm and hardware for the tessellation of polynomial surfaces. While conventional forward difference-based tessellation is subject to round off

error and cracking, our algorithm produces a bit-for-bit consistent triangle mesh across multiple independently tessellated patches. We present tessellation patterns that exploit the efficiency of iterative evaluation techniques while delivering a defect free adaptive tessellation with continuous level-of-detail. We a ...

Keywords: CAD, curves & surfaces, geometric modeling, graphics hardware, hardware systems, rendering hardware

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